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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,807	02/12/2004	Dae-Gunn Jei	678-1315 (P11491)	5842

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EXAMINER	
BROWN, VERNAL U	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,807	JEI ET AL.	
	Examiner	Art Unit	
	Vernal U. Brown	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-10, 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to communication filed on July 10, 2006.

Response to Amendment

The examiner has acknowledged the cancellation of claims 11-13.

Response to Arguments

Applicant's arguments filed 7/10/2006 have been fully considered but they are not persuasive.

Regarding applicant's argument regarding the power block, Kuttruff et al. teaches a power block EMP, comprising rectifier and voltage regulator (figure 2) and connected to the processing unit via the detection unit and the demodulators.

Regarding applicant's argument on page 10 regarding the RFID data with mobile protocol data, Kuttruff et al. teaches a storing protocol data which represent criteria for changing over transmission and the RFID data for controlling the modulators, encoders, and decoders are stored in the EEPROM (paragraph 056)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662.

Regarding claims 1 and 14-15, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L, L2) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and a second clock generator connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate of a first and second clock for the receive and

transmission part of the RFID device (figure 2) and one skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2).

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor and a second clock generator connected to the first clock generator, the codec, and the modulator in Kuttruff et al. because this enables the RFID device to clock the receive and transmitting section of the RFID device separately for facilitating the different transmission and reception rates.

Regarding claim 2, Kuttruff et al. teaches the processor extracts the RFID data from the memory portion (paragraph 040) in response to information indicating the approach of the RFID reader, provided from the detector, and delivers the extracted RFID data to the codec (paragraph 0036).

Regarding claim 5, Kuttruff et al. teaches a rectifier for rectifying a voltage detected from a signal received via the antenna and delivering the rectified voltage to the processor (paragraph 0052).

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 and further in view of Pratt et al. 20040198233.

Regarding claims 3-4, Kuttruff et al. teaches the detector generating a signal to the processor (paragraph 0039) but is silent on teaching the detector includes an interrupt port to the processor. Pratt et al. in an art related RFID device teaches the signal detected by a detector

circuit connected to the interrupt port of the processor for enabling the processor to enter in an active mode (paragraph 0045). Pratt et al. also teaches a frequency detector for detecting the received frequency (paragraph 0048).

It would have been obvious to one of ordinary skill in the art for the detector to include an interrupt port to the processor in Kuttruff et al. because this enables the processor to be transformed into an active mode upon detecting a received signal from the interrogator.

Claims 6-7and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 and further in view of Twitchell Jr. US Patent Application Publication 20050215280.

Regarding claims 6-7 and 16-19, Kuttruff et al. teaches a mobile terminal circuit for transmitting radio frequency identification (RFID) data to an RFID reader, comprising: an antenna (inductor coil L, L2) for communicating with the RFID reader (paragraph 0031); a memory portion for storing the RFID data together with mobile terminal protocol data (paragraph 0056); a codec COD1 for encoding the RFID data into RFID codec data (paragraph 040); a modulator MOD1 connected to the codec, for modulating the RFID codec data into RFID modulation data (paragraph 040); a processor VE connected to the memory portion, for extracting RFID data stored in the memory portion and delivering the extracted RFID data to the codec (paragraph 0056); a detector DE connected to the antenna and the processor, for informing the processor of an approach of the RFID reader (paragraph 0048). Kuttruff et al. teaches a power block comprising rectifier and voltage regulator (figure 2). Kuttruff et al. is silent on teaching a first clock generator connected to the processor and the memory portion, for providing operation timing to the processor and the memory portion; and a second clock generator

connected to the first clock generator, the codec, and the modulator, for providing operation timing to the codec and the modulator and is also silent on teaching the processor commands the power block to provide electric power to the RFID module. Ohkawa et al. in an art related RFID device invention teaches a RFID device having a first clock generator (61) connected to the processor 8 and the memory of the processor and teaches a carrier signal generator (62) connected to the first clock generator and the modulator 64 (figure 2). The carrier signal is used as a clock signal (figure 3). Although the reference of Ohkawa et al. is silent on teaching the second clock is connected to the encoder, the reference teaches the use of a separate of a first and second clock for the receive and transmission part of the RFID device (figure 2) and one skilled in the art recognizes that the encoder and the modulator forms the transmission path in the RFID device as evidenced by Kuttruff et al. (figure 2). Ohkawa et al. is also silent on teaching the processor commands the power block to provides electric power to the RFID module. Twitchell Jr. in an art related tag system invention teaches a processor commanding the power block to supply power to the RFID device (paragraph 0065) in order to conserve power when the device is not in use.

It would have been obvious to one of ordinary skill in the art to have a first clock generator connected to the processor and the memory of the processor and a second clock generator connected to the first clock generator, the codec, and the modulator and the processor commands the power block to provides electric power to the RFID module in Kuttruff et al. because this enables the RFID device to clock the receive and transmitting section of the RFID device separately for facilitating the different transmission and reception rates. The controlling of the power supply by the processor allows the conservation of the power supply.

Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 in view of Twitchell Jr. US Patent Application Publication 20050215280 and further in view of Jenkins, IV. et al. US Patent 6172518.

Regarding claim 8, Kuttruff et al. in view of Ohkawa et al. in view of Twitchell Jr. teaches the use of a processor to control the input power to the RFID module (see response to claim 7) but is silent on teaching the processor commands the power block using an enable pin. Jenkins, IV. Et al. teaches the conventional practice of using a power enable pin on a module to control the supply of power to the module (col. 2 lines 37-50) in order to conserve on the power supply.

It would have been obvious to one of ordinary skill in the art to command the power block using an enable pin because this provides an effective means of controlling the power supply base on external condition to the module in order to conserve on the power consumption.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 in view of Twitchell Jr. US Patent Application Publication 20050215280 and further in view of Applicant's Admitted prior art.

Regarding claim 9, Kuttruff et al. teaches a detector DE attach to the processor for detecting the received signal (paragraph 011) but is silent on teaching the detector is included in the processor. The applicant admitted prior art (figure 3) teaches a detector 307 integrated in a processor 100.

It would have been obvious to one of ordinary skill in the art to include the detector into the processor because this represents a cost saving by having fewer parts on the circuit board.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Ohkawa et al. US Patent 6972662 in view of Twitchell Jr. US Patent Application Publication 20050215280 and further in view of Pratt et al. 20040198233.

Regarding claim 10, Kuttruff et al. teaches the detector generating a signal to the processor (paragraph 0039) but is silent on teaching the detector includes a frequency detector for detecting a variation in frequency interrupt port to the processor. Pratt et al. in an art related RFID device teaches a frequency detector for detecting the received frequency (paragraph 0048).

It would have been obvious to one of ordinary skill in the art for the detector to include a frequency detector for detecting a variation in frequency this allows the proper demodulating and decoding scheme to be used to capture the received data.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttruff et al. US Patent 20020080864 in view of Twitchell Jr. US Patent Application Publication 20050215280.

Regarding claim 13, Kuttruff et al. teaches a processor for controlling the receipt and transmission of data (paragraph 0031) but is silent on teaching the processor commands a power block to provide electric power to the RFID module upon detecting the approach of the RFID reader. Twitchell Jr. in an art related tag system invention teaches a processor commanding the

power block to supply power to the RFID device (paragraph 0065) in order to conserve power when the device is not in use.

It would have been obvious to one of ordinary skill in the art for the processor to command the power block to provide electric power to the RFID module upon detecting the approach of the RFID reader because this allows the conservation of power.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vernal U. Brown whose telephone number is 571-272-3060. The examiner can normally be reached on 8:30-7:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 571-272-7308. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vernal Brown
September 25, 2006

BRIAN ZIMMERMAN
PRIMARY EXAMINER